Design for Manufacturing

By
Kirti Sikri Desai

Abstract

In the past, the design and manufacturing worlds were considered very separate and distinct entities. In the ongoing drive towards smaller, faster and cheaper chips, the worlds of design and manufacturing are colliding. Design for Manufacturability (DFM) and Design for Yield (DFY) have emerged as major drivers as the semiconductor industry continues on its historic scaling trend.

The purpose of this article is to explain what problems are cropping up for designers and foundries, as geometries shrink to 90-nm and 65-nm technology nodes, why these problems will become even more significant with future nodes, what is DFM, how are EDA companies responding to DFM challenge.
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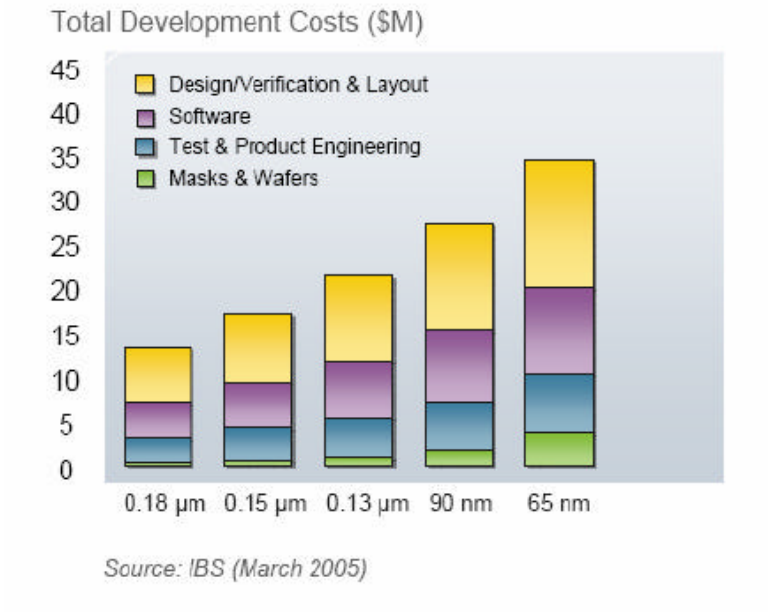
1.0 Foundries

Pure-play foundry has been one of the most successful innovations in the semiconductor industry. Twenty years ago, these independent foundries didn't exist.Their success has rippled through the industry, giving rise to fabless design firms and the customer-owned tooling (COT) do-it-yourself design revolution, in which a customer hands a finished chip design to its foundry. In 2004 the combined revenues of the four largest foundries—**Taiwan Semiconductor Manufacturing Company** (TSMC), **United Microelectronics Corp.** (UMC), **Chartered Semiconductor Manufacturing** and **Semiconductor Manufacturing International Corp.** (SMIC) exceeded $14 billion.

As semiconductor features shrink in size and pitch, the challenge of ramping manufacturing up to acceptable yields and within reasonable timeframes increases dramatically. In the past, designers were shielded from the intricacies of the fabrication process by the use of “design rules” and “recommended rules” provided by the foundry. . In the case of today’s ultra-deep submicron technologies, however, these rules no longer reflect the underlying physics of the fabrication process. Increasing variability, mask cost and data explosion, and lithography hardware limitations are posing significant design challenges for the manufacturability of integrated circuits In the ongoing drive towards smaller, faster and cheaper chips, the worlds of design and manufacturing are colliding.



Costs of developing a chip has been increasing as shown in Figure 1. "*If you're working at 90 nanometers or 65 nanometers, it's probably going to cost you 20 to 30 million dollars to get your chip on the market*," says Risto Puhakka, vice president at VLSI Research. Why are designs becoming so pricey? The short answer leads us right back to ***Design for Manufacturing*** (***DFM***)

Despite its obvious success, the basic foundry business model is about to change. The cost of developing and building a state-of-the-art manufacturing process has ballooned to the point where only the very largest foundries can consider the investment. At the same time, the high cost of developing chips for the newest fabs has design firms clamoring for design-for-manufacturing tools that break the traditional barrier between design and manufacturing.

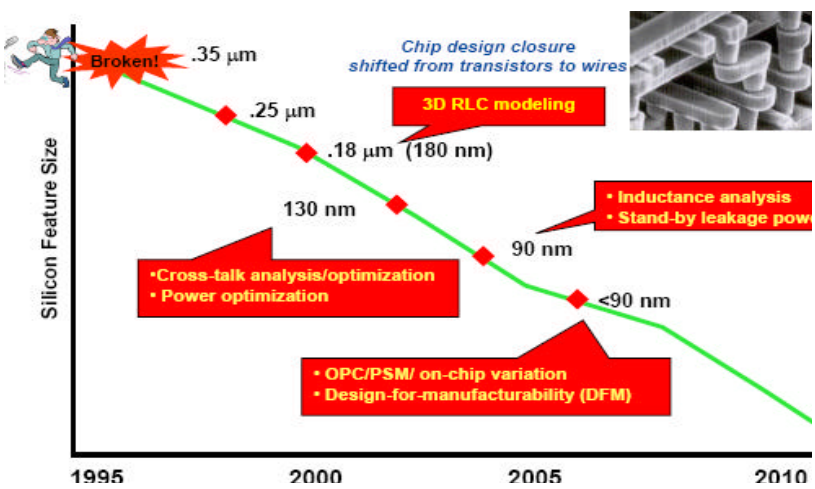
Figure 1: Development Cost of Chip at different technologies.

2.0 Shrinking Geometries

Designs are moving to smaller geometries. Designs are moving from 300nm, 130nm, and 90nm to 65nm, 45nm geometries. As geometries shrink number of gates increases. Shrinking geometries crops up new design problems. Let us look at the problems faces by designers because of shrinking geometry.

2.1 Designers and Shrinking Geometries

In the late 1980's, a chip design contained approximately 20,000 gates. The average design team used a logic synthesis tool to sign off



a register transfer level (RTL) database before sending it to an ASIC vendor for physical implementation. This resulted in a chip that performed as expected.
In the 1990's, as the geometry shrank to 180 nm the number of gates crossed million. With gate count moving closer to one million, interconnect delay became a significant factor in total chip timing. Designers of a typical 250nm chip, consisting of an average 7.5 million gates, were concerned with optimizing timing and area. Design teams signing off on an RTL database found longer and longer delays in getting chips back from their ASIC manufacturer – and even then, they might not perform as expected. To deal with these problems, more design teams brought physical implementation in-house – using a whole new set of physical synthesis tools provided by their electronic design automation (EDA) vendors.

Figure 2: Shrinking geometries and Problems

At 130nm and 55 million gates, signal integrity got added to the list of implementation issues that must be addressed. With the advent of the advanced 90nm and 65nm processes for IC design, semiconductor process variation is much more of an issue, and leakage current dominates the power budget. Figure 2 shows the problems due to smaller geometries.

2.2 Manufacturing and Shrinking Geometries

1) Resolution: The features (structures) on the silicon chip are now smaller than the wavelength of the light used to create them (Figure 3). This is akin to trying to pain 1/4-inch wide line using a 1-inch diameter paintbrush.
If we assume that the green geometric shape shown in the Figure 3 is the ideal (desired) form, then this is the shape that would be created in the initial GDSII file generated by the physical design tools. The problem is that if this shape is subsequently created as-is in the photomask, then the corresponding form appearing on the silicon would drift farther and farther from the ideal as feature sizes associated with the newer technology nodes decrease.

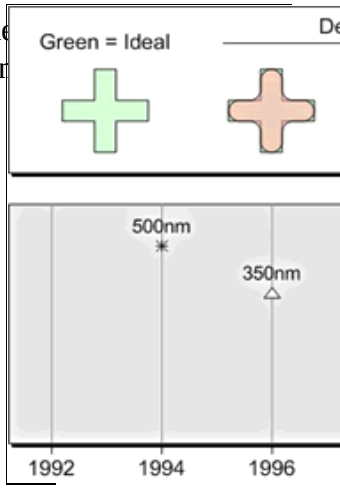
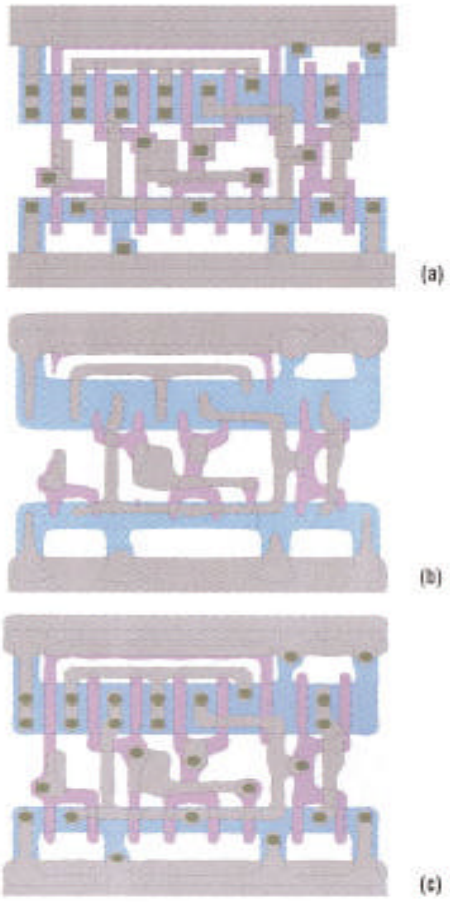


Figure 3:What you

The way this is currently addressed is to post-process the GDSII file with a variety of ***Resolution Enhancement Techniques (RET)***, such as ***optical proximity correction (OPC) and phase shift mask (PSM).*** In the case of OPC, for example, the tool modifies the GDSII file by augmenting existing features or adding new features – known as sub-resolution assist features (SRAF) – to obtain better printability. If we know the printing process will be distorted in a particular way, then we can add our own distortion in the opposite direction in an attempt to make the two distortions cancel each other out as shown in Figure.

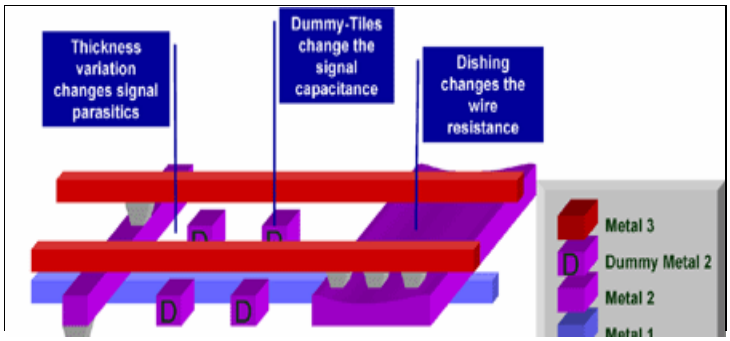


1. Today's DFM approaches are largely post-GDSII operations. The effects of RET can be seen in the differences between a 90-nm design layout (a), the printed result without RET (b), and the same printed result after application of RET (c). (courtesy of Mentor Graphics)

The problem is that every structure in the design is affected by its surrounding environment in the form of other structures in close proximity. If the same shapes are located in close proximity to each other, interference effects between the light used to create these shapes will modify each shape, often in non-intuitive ways. The end result is that every aspect of the design, down to the timing and reliability of each cell and track – is strongly affected by the placement and routing of the design.

2) Processes like chemical/mechanical polishing: ***Chemical and mechanical polishing (CMP)*** has been a standard part of the manufacturing process for multiple generations. It is used to keep a lithography surface flat (or planar) – including both aluminum and copper metallization. CMP can cause substantial variation in interconnect thickness across the wafer and even the die. When designers model their interconnects, they usually assume a constant thickness. At the 65-nm process node, CMP removal rates are a function of local interconnects density. Therefore, CMP will create thickness variations of the inter-metal dielectric or of the copper interconnects and hence in resistance and capacitance, of up to 40% versus what they modeled. .

To avoid these problems, many manufacturers began to insert dummy metal fill to even out the interconnect pattern density. The dummy metal fill, consisting of tiles in empty areas of chips, is inserted in a post-processing step as shown in Figure 4.



However, metal fill affects chip timing, signal integrity

and even functionality. Tight control of planarity requires dummy tiles to be placed in close proximity to functional features. This may cause coupling with functional wires – and creates additional parasitics. The existence of the tiles changes capacitance. CMP dishing changes wire resistance, and dielectric thickness variations also change signal parasitics Originally, this planarization was a yield enhancement technique today, however, CMP can pose a yield challenge.

Figure 4: CMP

Manufacturing and yield problems typically fall into four main categories as illustrated below.

	Catastrophic	Parametric
Systematic (Feature-Driven)	Feature/Layout-driven shorts and opens	Feature/Layout-driven impacts on timing/power/noise...
Statistical (Random)	Random shorts and opens (e.g. a via not printing)	Statistical (process-related) impacts on timing/power/noise...

Catastrophic problems are those such as a missing via, which will cause the chip to fail completely. By comparison, parametric problems leave the chip functioning, but out of its specified range, such as a 500 MHz device that runs at only 300 MHz or a part that consumes 8W of power when it is required to consume less than 5W. The origins of both catastrophic and parametric problems can be sub-divided into systematic (feature-driven) effects and statistical (random) occurrences.

3.0 What is DFM?

Current ruminations about DFM in various forms are reminiscent of the fable of three blind men attempting to identify an elephant. With 25+ EDA companies offering DFM products, it seems that DFM means different things to different people. DFM product offerings now include

- Reticle enhancement technology (RET), such as optical proximity correction (OPC) to address limits of lithography. It also includes products to improve OPC results.
- There are products to address chemical mechanical planarization (CMP) limits of the fabrication process.
- DFM aware routers that improve manufacturability and yield by considering more of the manufacturing process during their execution.
- There are products to post-analyze layout and routing for manufacturability.
- DFM solutions are offered for analysis of random defects in fabrication on yield, and emerging are solutions for analyzing the effects of parasitic variations, resulting from process variations, on yield. With these yield solutions is emerging the development of statistical design and analysis tools pushing the DFM scope into other classical EDA areas such as (statistical) timing analysis.

However, the mixed bag of different problems being addressed by the “DFM” companies seems to justify a definition for DFM as being “anything and everything relating to the design of a chip” to be manufactured. DFM is also referred as “Design For Marketing”, “Dollars for me”

4.0 Fabs & DFM.

As design processes have continued to shrink to 90 and 65 nm, lithography, mask-making, and fabs have become even more reliant on EDA-vendor inventions and fixes in design tools to ensure the accurate manufacture of chips. Three biggest foundries employing 65-nm processes—TSMC (Taiwan Semiconductor Manufacturing Co), UMC (United Microelectronics Corp), and the CIS (Chartered/IBM/Samsung) Alliance—have all added a number of DFM technologies to their reference flows, for example, TSMC 7.0 reference flow in Figure 5. In doing so, they are putting some of the burden to improve fabrication quality and yield on designers

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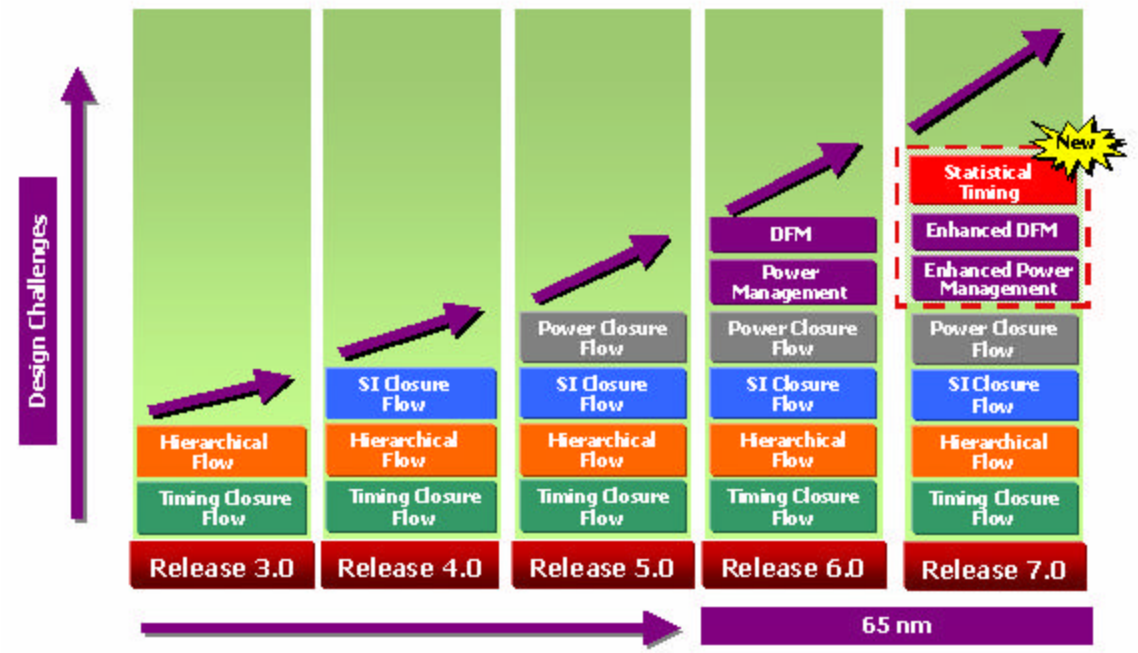

Figure 5: TSMC 7.0 Reference Flow

TSMC Reference Flow 7.0 provides extensive solutions to the 65nm design challenges. The new Reference Flow includes major enhancements in the areas of power management and design for manufacturing to reduce power consumption and maximize yield. In addition, statistical timing analysis is introduced for the first time, enabling designers to optimize the design margin and yield through accurately analyzing process variation impact on timing.

For years, TSMC has been driving the big vendors to ensure that their tools support its 65-nm process. The foundries are meeting the DFM challenge head on, by creating closer relationships with their customer base. From TSMC Web site designers can obtain detailed information about TSMC's manufacturing processes. UMC also collaborates closely with design firms "early and often throughout the rest of the semiconductor supply chain

A couple of years ago, foundries were less than willing to share their sensitive defect density, yield data, and lithography models with EDA vendors, especially start-ups, fearing that the data would end up in competitors' hands. For example, TSMC recognized that sharing data with EDA vendors would be essential to the success of 65-nm silicon and EDA-DFM-tool development. TSMC has unveiled its DDK (DFM Data Kit) and DUF (DFM Unified Format), which encapsulate data for LPC (lithography-process check), CMP (chemical-mechanical-polishing) analysis, and CAA (critical-area analysis). Devising this common format allows TSMC to work more closely with established EDA vendors but also provide up-and-coming tool vendors in the EDA market with solid data to try to make their tools comply with TSMC's 65-nm flow
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5.0 EDA and DFM

Estimates for the size of the DFM market are hard to come by, partly because the industry has yet to come to consensus about what exactly encompasses DFM, and partly because many companies in the space are smaller startups that do not disclose revenues. Canaccord Adams and Mentor have come up with up various segments in DFM and DFM market share.

5.1 Canaccord Adams DFM View [2]

As per Canaccord Adams, a Canadian financial services company, the market for design-for-manufacturing technology is currently worth between $350 million and $400 million. It carves DFM into three slices.

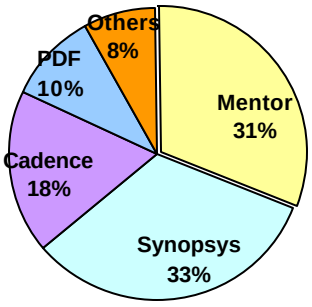
- "*Manufacturing-process-aware chip design*," which includes design tools that specialize in helping designers account for manufacturing conditions and process variations;
- "*Resolution enhancement technologies,"* techniques such as optical proximity correction (OPC) and phase-shift mask (PSM) that help lithographers "trick" light to print sub-resolution features using 193-nanometer lithography; and
- "*Process characterization and yield analysis*," including tools to analyze manufacturing yields as well as test-driven technologies

Manufacturing-process-aware chip design tools make up by far the smallest portion of the DFM market, currently about $50 million annually. The RET market is currently worth more than $150 annually, and the process characterization and yield analysis market is about $160 million, including TCAD software.

5.2.Mentor Graphics Corp.'s DFM View [5]

As per Mentor Graphics, DFM can be broken into three segments:

- "*old school*" technologies such as design rule checking, parasitic extraction and TCAD;



- "*manufacturing-for-design*" technologies like RET and verification; and
- "*design-focused" technologies* like lithography and yield analysis tools.

The DFM market was worth about $700 million in 2005, consisting almost entirely of revenue generated by the old school and manufacturing-for-design categories, Under Mentor Graphics, definition of DFM, Mentor owned 31 percent of the market in 2005, with Synopsys Inc. holding 33 percent and Cadence Design Systems Inc. holding 18 percent as shown in Figure 6

Mentor Graphics forecasts the market to grow to more than $800 million this year. Revenue from design-focused technologies will not start to make a significant impact until next year, according to analysis.

Figure 6: Market share of DFM as per Mentor

By 2010, the DFM market will be worth more than $1.5 billion, according to analysis, of which only about $100 million will come from the design-focused category.

5.3 DFM Companies:

A list of "DFM" companies and their tools.

Company	DFM Field	Tools
Cadence http://www.cadence.com/	Physical verification and sign-off electrical verification	Physical Verification System, Assura DRC Assura LVS Cadence Chip Optimizer Cadence QRC Extraction Diva Physical Verification Dracula Encounter Test PacifiX Staic Noise Analyzer Virtuso RET Suite
Synopsys (acquired Sigma-C) http://www.synopsys.com/	RTL to Silicon Mask Synthesis Mask Data Preparation LithographyVerification TCAD Design for Yield	Prime Yield Tool Suite Hercules PSM-Create Proteus IC Workbench SiVL CATS TCAD Galaxy Design Discovery Verification
Mentor Graphics http://www.mentor.com/	OPC, RET	Calibre nmOPC Calibre OPCverify Calibre LFD: Litho-Friendly Design Calibre RET (OPC and PSM)

		Calibre MDP Calibre nmDRC
Magma http://www.magma-da.com//	Chemical mechanical polishing, lithography simulation	Talus DFM, Quartz DRC QuartzLVS
Nannor Technologies http://www.nannor.com		*Acuma*, a post routing optimization tool that implements recommended design rules for manufacture closure and that optimizes layout for yield improvement.
Clear Shape Technologies http://www.clearshape.com/ Model-based DRC tool. Extreme DA	Full-Chip Design Manufacturability Checking and Fast Silicon-Accurate Contour Shape Electrical DFM Analysis and Optimization Solution	InShape, OutPerform
Blaze DFM (acquired Aprio Technologies) http://www.blaze-dfm.com/	Electrical DFM solutions addressing the issue of parametric yield	BlazeIF, a dedicated fill synthesis solution. Blaze MO, which performs power and timing optimization of a finished design just prior to the handoff to manufacturing Aprio has Halo-Fix, an automated OPC repair tool, and Halo-Quest, which provides lithography variability analysis for designers
Ponté Solutions http://www.pontesolutions.com/	critical area analysis and yield sensitivity analysis	Yield modeling and yield analysis.
Predictions Software http://www.icyield.com/		*EYES*, a tool for making integrated circuit yield predictions; *PEYE-CAA*, which provides the ability to generate and display critical areas of an IC layout; *PEYE*, a layout modification/analysis tool for the automation of yield and reliability enhancement.
Pyxis Technology http://www.pyxistech.com/		Routing software for sub-100-nm processes that targets yield, lithography, and manufacturability at the design phase.
PDF solutions http://www.pdf.com/		Integrated Yield Ramp solutions Design-Based Yield Improvement solutions
Sagantec http://www.sagantec.com/		SiFix, which detects and corrects physical violations in technology and reliability design rules; XTREME,

		which re-engineers chip interconnect wires to reduce coupling capacitance, crosstalk, and critical net loads to enhance signal integrity, reliability, and yield; and DFM-Fix, a tool that automatically optimizes design tape-out data to eliminate lithography related hot spots.
Silicon Design Systems http://www.silicon-value.com		K-Route placement-independent interconnect synthesis, which simultaneously uses routing, extraction, analysis and optimization engines.
Stratosphere Solutions http://www.stratosol.com		StratoPro, IP that supports DFM and DFY through process characterization.
Virage Logic http://www.viragelogic.com		FirstPass-Silicon Characterization Lab, which helps ensure reliable IP across a range of foundries.
XYALIS http://www.xyalis.com		Software targeting design for manufacturing and mask preparation GTViewer, GDSII database viewer GTTiler, high performance "dummy" tiles generator GTmuch, Multi Chip Project editor GTcheck, GDSII databases integrity verifier GTmerge, GDSII databases merging tool GTsuite, XYALIS layout finishing tools GTsmooth, Hybrid metal-fill tool

6. Conclusion

As silicon-manufacturing effects impact design success more heavily, it is the next evolutionary step for design teams to look to their EDA vendors for tools that will embed manufacturing and yield effects into the design flow. And it is the next evolutionary step for EDA vendors to build the partnerships with manufacturers and equipment companies in order to provide these solutions. With new approaches, design and manufacturing groups can reduce design data volume and mask cost, improve the performance of designs, and enable more efficient chemical and mechanical polishing (CMP).

DFM is centered on the relationship between design and manufacturing. However, it ultimately affects and is influenced by areas across the entire high-tech supply chain. *DFM is all about the link between design and manufacturing. One needs to fuse these*

two disciplines together to improve the quality of chip. Aim is to *design chips that can be physically manufactured and work as planned. "The DFM market is growing very well — far more than the EDA market is growing overall*,"

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3. ESNUG post 453, http://www.deepchip.com/posts/0453.html
4. Business of DFM: http://www10.edacafe.com/nbc/articles/view_weekly.php?articleid=285249