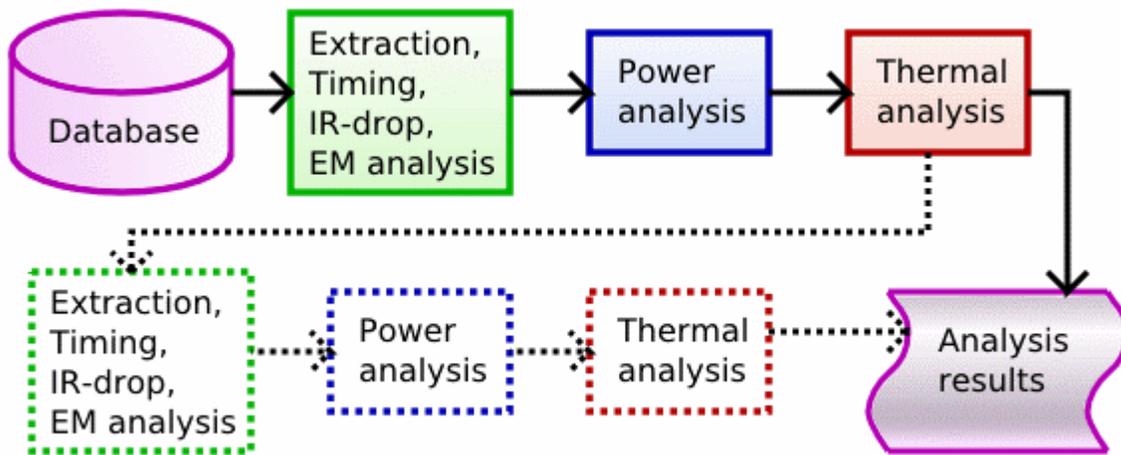


# Invarian Addresses Sign-Off Predictability Issues With Concurrent Analysis For Power, Voltage, Temperature, And Timing

Alex Samoylov, Invarian

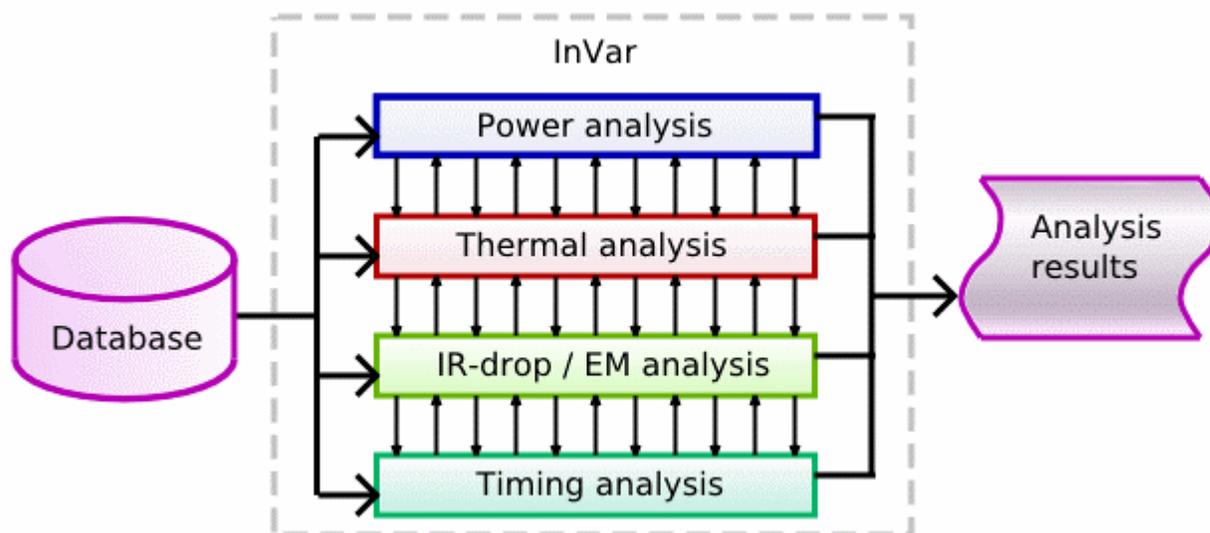
IC designers responsible for the physical implementation of the design face a huge problem of design sign-off analysis. Today, they need to use different tools to verify the various design aspects, such as timing, power, voltage drops, and chip temperature. The problem is that each of these analyses needs the results of all the other analyses. Therefore, typically, these tools are run sequentially in a flow, so that the results of one tool can feed the next tool. This flow is then run multiple times, each time using the results of the previous iteration. The steps in the typical sign-off analysis flow are shown in **pic. 1**.



**Picture 1. Typical sign-off analysis flow**

This approach has several problems. First, because of the iterative approach, it is a highly inefficient use of expensive computing resources. Second, this flow may only converge slowly, but often, because of required compute resources and long run times, only a few iterations are run. Third, not all analysis tools take package characteristics into account. Finally, again because of the cost and run time, these analyses are not run across enough process corners to reliably predict the design performance across all process variations.

*InVar*, the first tool that implements concurrent co-simulation (co-analysis) for power, timing, temperature, and IR drop, addresses the predictability and reliability issues of the current analysis flows. Multiple engines running in parallel on the same design data with continuous feedback between them better represent the real physical processes within the design. Power dissipation, heat transfer, and voltage drop in a real chip occur simultaneously, not sequentially.



**Picture 2. Sign-off analysis flow with *InVar* : One tool, one run.**

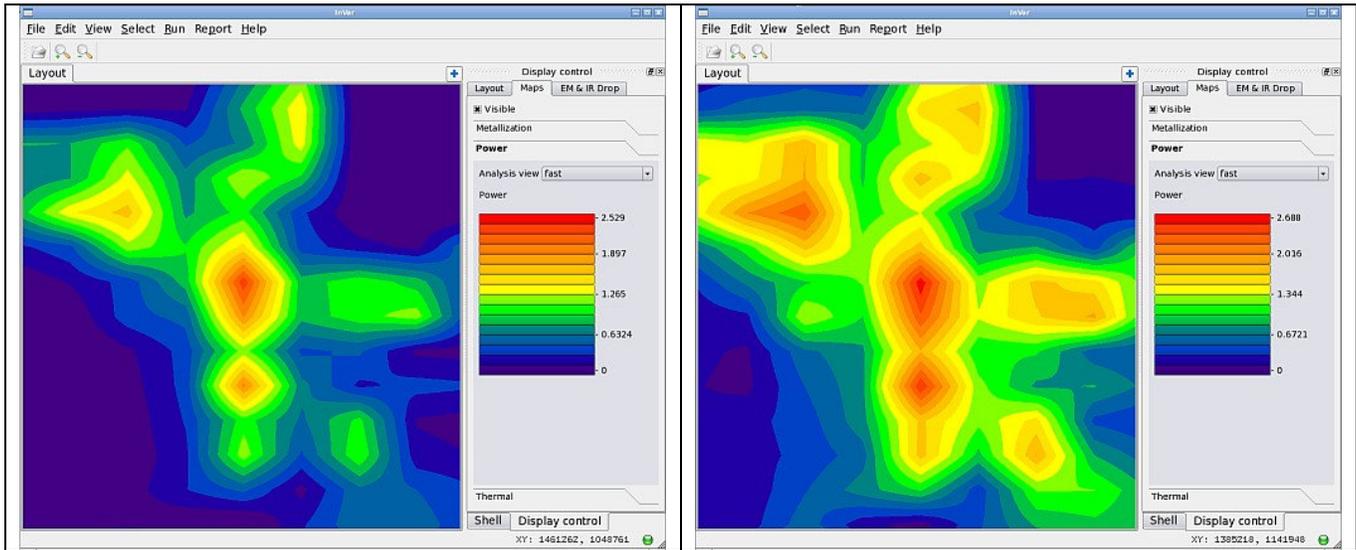
Experiments with *InVar* have demonstrated the stability and fast convergence of this approach. *InVar* is concurrent by nature and supports both multi-threading and multi-processors.

*InVar* can also run all analysis engines separately and mimic traditional analysis tools. When the results of a concurrent run versus a sequential run are compared, various effects impacting each other could be observed:

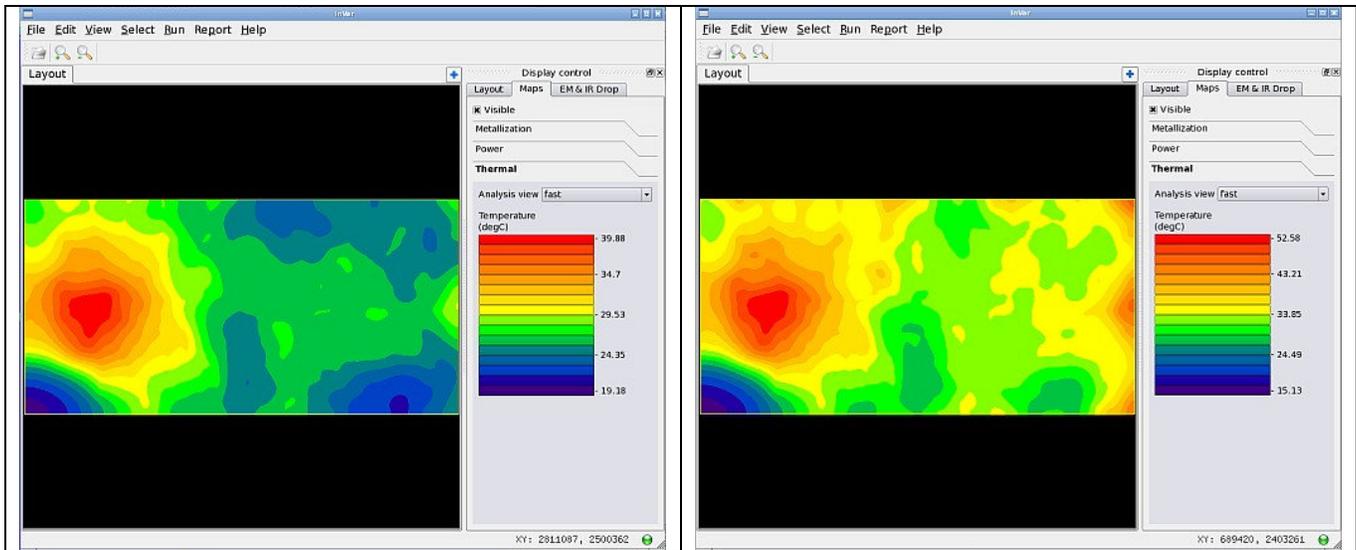
- Leakage power increases with temperature.
- Cell-switching power decreases at higher temperature with fixed input transition.
- Delay and transition times increase with temperature.
- Increase in power increases voltage drop.
- Wire resistance increases with temperature.

All these dependencies are very complex, and determining their combined effect from **separate analyses** is very difficult.

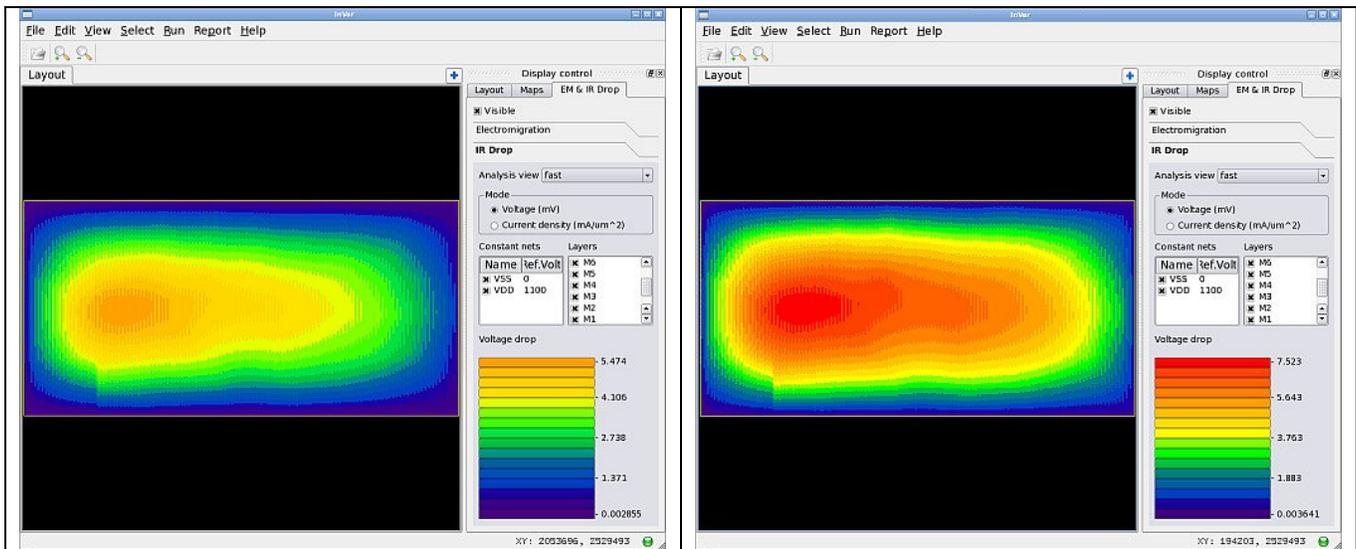
## Conventional vs. Concurrent analysis examples



Picture 3. Power density – conventional analysis is on the left.



Picture 4. Thermal analysis reveals higher temperature along with higher temperature variability.



**Picture 5. Same voltage drop is represented by the same color; concurrent analysis is on the right.**

In this design, concurrent co-simulation shows a 15% increase in power consumption compared to the traditional approach. One can also note the following differences in the analysis maps:

- Power density obtained by the conventional flow is more uniform, but co-simulation reveals areas of greater power density. Local peak power density in co-simulation mode is almost 60% higher.
- Thermal variability in the temperature map significantly increases; local areas become hotter.
- Changes in temperature and power cause changes in IR-drop. In co-simulation, much higher voltage drop occurs in local areas.

**Aforementioned effects are not a “rule of thumb.”** Power, temperature, and voltage drop in concurrent analysis highly depend on package characteristics defined in input data and environment conditions. They may increase and decrease compared to the results of simple analysis techniques. Concurrent co-simulation reveals the higher variability of operating parameters across the chip, and variability seriously affects WNS while TNS, which is an integral characteristic, barely changes.

Without co-simulation, analysis results are overly optimistic. Local areas where temperature, power, or voltage drop deviate from the average can be easily overlooked but can cause functional, timing, and yield problems in production phase.

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Contact: Alex Samoylov, Invarian, (408)-834-5942, Email: [ales@invarian.com](mailto:ales@invarian.com), <http://invarian.com>