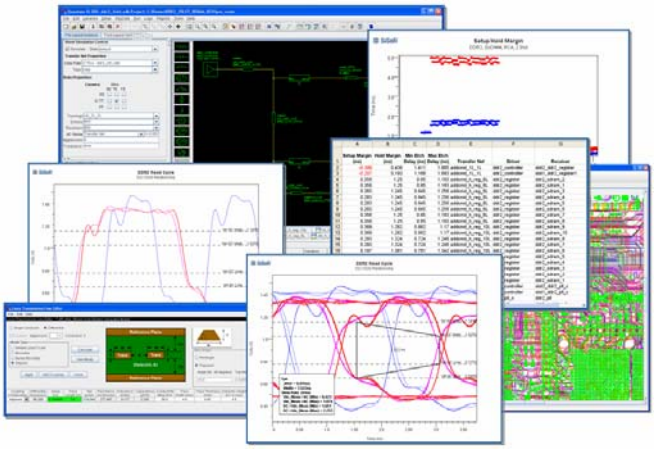
Quantum-SI™

Integrated Static Timing, Signal Integrity and Crosstalk Analysis



Overview

Quantum-SI™ integrates timing, signal integrity and crosstalk analysis to determine voltage and timing margins for high-speed system designs. Quantum-SI automates both pre-layout and post-layout analysis, allowing designers to quickly achieve High-Speed Design Closure™. Advanced modeling and simulation capabilities predict system-level noise and timing margins more quickly and accurately than traditional signal integrity tools.

Interface-centric Analysis

Quantum-SI analyzes an entire high-speed ***interface*** for both signal integrity and timing. Topologies for different net classes (transfer nets) are captured using a schematic editor that allows different net classes to be edited concurrently. Design-specific analysis settings (clock speeds, data rates, stimulus patterns, transaction-dependent simulation models, timing reference points and valid driver/receiver combinations) are also captured at this stage. Quantum-SI uses this information to automate SI analysis & interconnect delay extraction for all the signals in the interface. Extracted interconnect delays are automatically combined with component timing information to establish timing margins.

Flexible, Accurate Modeling

Quantum-SI allows designs to be modeled at varying levels of detail, depending on the interface's operating speed and margins. IBIS models provide base information for each component and reference more detailed models where required. I/O buffers can be modeled at the behavioral or transistor level.

Multiple package modeling styles are supported, including IBIS, SPICE subcircuit and S-parameter descriptions. Quantum-SI automatically creates models for lossy transmission lines and vias, which can be overridden to use models based on external solvers or measurement.

Timing models define component output timing and input setup / hold requirements. Advanced models adapt timing values automatically based on clock speed. Dynamic timing models support adaptive timing technologies like DDR3 write leveling by describing the device's self-optimizing behavior.

Accurate noise modeling is a key requirement for accurately assessing system operating margins. Quantum-SI employs a unique pre-/post-layout methodology for modeling switching noise and crosstalk that allows noise budgets to be established early in the design cycle and rapidly validated after layout.

Integrated Pre-/Post-Layout Analysis

The Quantum-SI schematic editor is used to capture interconnect topologies for pre-layout simulations. Pre-layout analysis allows different termination schemes, I/O buffer selections and routing strategies to be quickly analyzed and assessed for their effect on overall interface margin. Swept-parameter analysis allows users to explore their design's sensitivity to varying circuit parameters. Quantum-SI automatically runs specified simulation cases, analyzes waveform quality, performs interconnect delay extraction, runs timing analysis and presents an integrated report with both signal integrity and timing results.

Quantum-SI provides superior post-route design analysis capabilities. Pre-route topologies are ***automatically*** mapped to actual routed nets, allowing users to set up post-route analysis within minutes. Quantum-SI automatically runs signal integrity, timing and crosstalk analysis and presents results in the same format as pre-route analysis, simplifying comparison of actual to expected results.

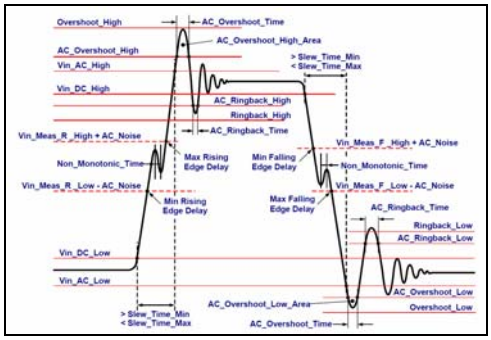
PCB databases from multiple CAD systems are extracted and managed using a graphical interface that guides users through the setup process. Extracted PCB databases can be reused across projects, allowing users to establish a library of reference board designs.

SiSoft™

Quantum-SI *(continued)*

Comprehensive Post-processing

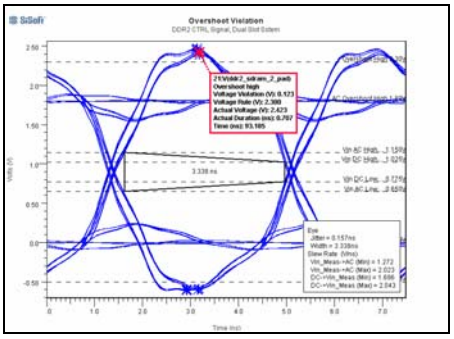
Generating thousands of simulation cases is easy, but extracting accurate waveform quality and interconnect delay information is not. Quantum-SI analyzes signals at the device pin, pad, or core using the most rigorous waveform processing in the industry. Every edge of every waveform is analyzed for waveform quality, slew rate, area and timing parameters. Interconnect delays are automatically normalized based on detailed driver and receiver component timing specifications.



The Quantum-SI timing analysis engine combines interconnect delays with component timing data to provide an integrated signal integrity and timing report. This report includes summary data for waveform quality and timing margins, accompanied by multiple levels of drill-down detail.

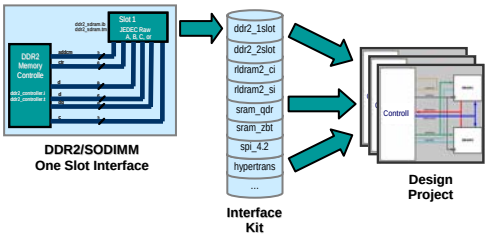
Advanced Waveform Viewer

SiViewer provides interactive display of simulation waveforms and results. Waveform data is presented in time-domain, eye diagram and bus (side-by-side) formats, with key waveform metrics displayed.



SI / timing analysis results can be displayed as scatter plots, showing how voltage and timing margins are distributed across an interface. Waveform quality violations can be highlighted on screen and examined in detail.

Quantum-SI Design Kits



Quantum-SI design kits can shave weeks to months off your next project by reducing model development and interface capture efforts. Design kits include validated timing and signal integrity models, transfer net topologies and analysis settings for standard interface technologies including DDR2, DDR3, QDR SRAM, RLDRAM, PCI-Express, SATA, USB2 and XAUI.

Quantum-SI design kits are available at multiple levels of customization, including:

- Architectural (technology-specific with generic components)
- Implementation (complete pre-route setups for specific combinations of components)
- Validation (complete pre-/post-route setups based on specific reference PCB designs)

Backed by SiSoft's Experience in High-Speed Systems Design

SiSoft's consulting services group uses Quantum-SI every day, analyzing the industry's most challenging designs. We have the experience to help you get your next design up and running quickly.

CAD layout system support

- Allegro®
- Expedition PCB™
- PowerPCB™
- Board Station®
- Pantheon®
- P-CAD™

Contact SiSoft
To learn more about SiSoft's products, contact sales@sisoft.com or visit our website at www.sisoft.com.