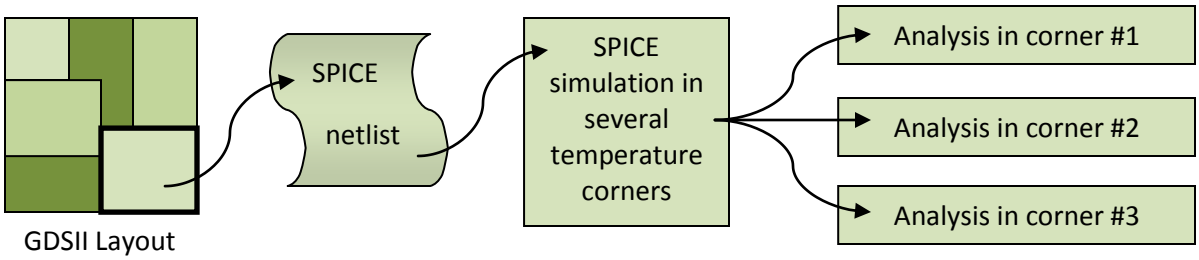
Temperature/Layout Aware Analog Sign-off

Analog IC designers face serious design sign-off and analysis problems with the increasing size of analog modules and higher integration levels of current SoC solutions. Traditional sign-off approaches do not include layout information and accurate temperature annotation for circuit components. In a typical sign-off flow, circuit analysis is performed with a layout-extracted netlist in several temperature corners. Most advanced flows include various Monte Carlo methods to account for random variability of parameters. The verification flow for analog blocks is linear in nature and typically does not include the whole SoC and packaging into analysis process.



Picture 1. Traditional analog sign-off simulation flow

There are several problems with this linear approach:

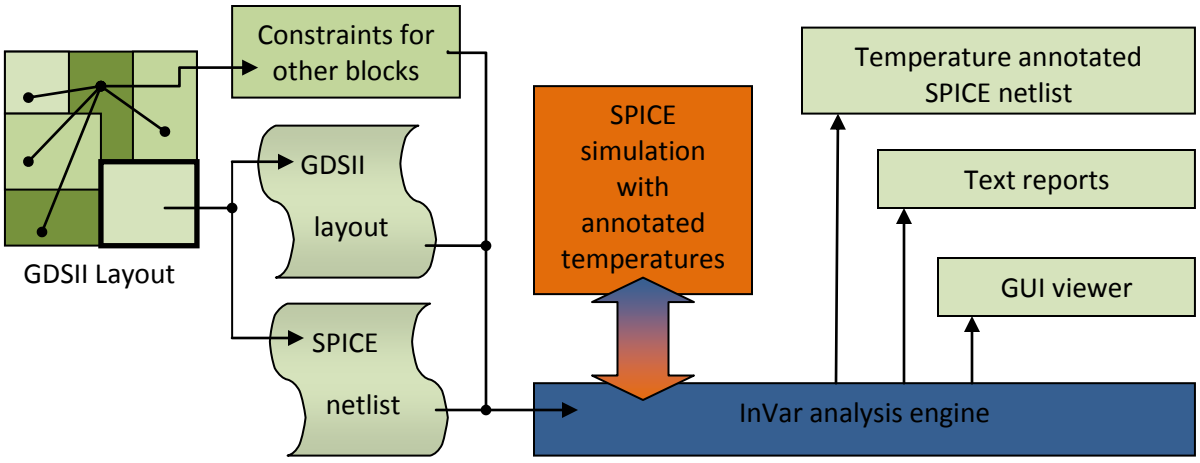
a) Temperature corners do not model actual temperature variability across the SoC
b) Surrounding blocks and their effect on temperature are ignored
c) Packaging and substrate parameters and their effect on temperature are ignored
d) Parameter variability (if any) does not model temperature gradients

In nanometer designs, high Tc numbers for diffusion and high temperature variability make temperature aware sign-off absolutely critical. InVar by Invarian addresses these challenges for analog blocks instantiated in SoC designs.

With introduction of analog design analysis functionality in **InVar 2.0**, the tool can perform accurate temperature/layout aware analog sign-off analysis with external circuit simulation engine. There are following benefits of joint solution:

a) Analysis becomes very accurate with actual temperature assigned to each component.
b) Accurate identification of electromigration issues
c) Mapping of SPICE netlist to layout provides accurate locations for hotspots
d) InVar solves **full 3D heat transfer equation** to assign temperature to design components. Input data to solve heat transfer problem includes block layout, temperature-dependent power of components, and power dissipated by other blocks in SoC design
e) It is very easy to simulate analog module(s) in SoC environment; only minimal input is required for other blocks

InVar 2.0 Flow



Picture 2. Analog sign-off simulation using InVar circuit simulation integration

To perform InVar 2.0 analysis, user should have available:

a) GDSII layout of analog module(s)
b) Source or extracted SPICE netlist(s)
c) SoC floorplan with placed blocks. User can estimate behavior of existing analog IP at:
    a. floorplanning stage
    b. tapeout stage
d) Power and metallization numbers for other blocks. Blocks could be divided into sub-blocks for accurate simulation of hotspots
e) Technology specific parameters like thermal conductivity, thickness, and package characteristics
f) Environment conditions

User can perform analysis for standalone analog modules as well; in this case, requirements c) and d) are optional.

In the process of data import, InVar performs state of the art mapping between the netlist and layout. This step is critical for accurate calculation of temperatures. Once mapping is done, the tool starts electro-thermal analysis with external circuit simulation engine.

In the process of co-analysis, InVar calculates the sustained temperature and power over a defined period of time. Flexibility in defining starting temperatures, input stimuli, and simulation time allows user to calculate average and dynamic peak temperatures as well. The tool can run on multiple threads on multiple CPUs. In case of multiple analog modules instantiated in SoC, the tool can utilize multiple circuit simulator and InVar licenses to avoid runtime degradation typical for sequential simulation runs.

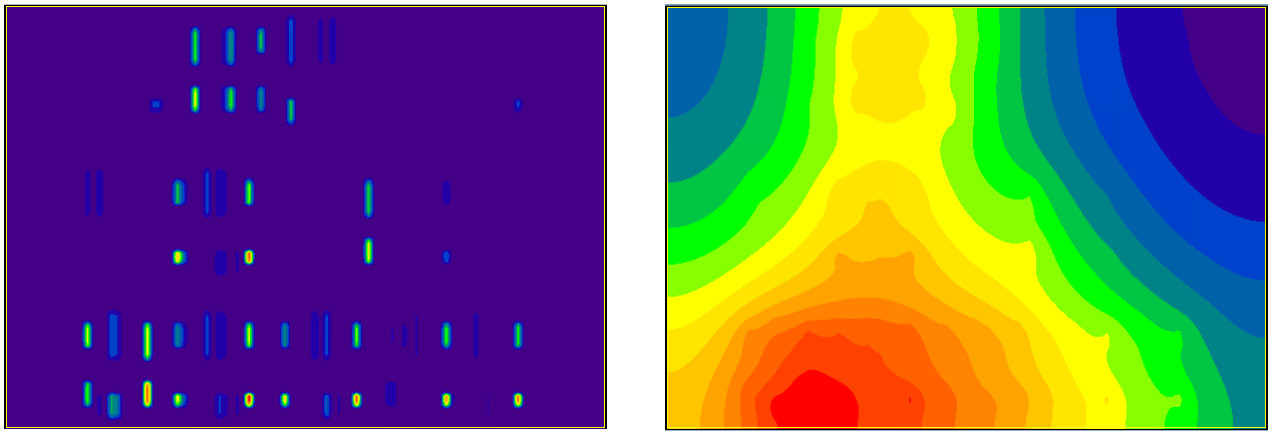
Implementation with the Analog FastSPICE Platform

The current implementation of InVar 2.0 uses the Analog FastSPICE™ (AFS) Platform from Berkeley Design Automation for circuit simulation. The AFS Platform always delivers nm SPICE accurate results, 5x-10x higher performance than traditional SPICE on a single core and has >10 million-element capacity. For circuit characterization applications, the AFS Platform delivers up to 50x higher performance than traditional SPICE on a single multi-core computer. AFS provides InVar 2.0, with the accuracy, performance, and capacity required for temperature/layout aware sign-off analysis.

Factors affecting accurate analysis

There are many factors affecting accurate analysis, but the most important are temperature dependent changes in SPICE models, effects of power dissipation in surrounding blocks, and package/die characteristics. Let us consider it by example. Sample design has three instances of the simple analog module and eight blocks in total. Design area is close to 15000μ^2.

Power and thermal maps for analog block



Picture 3. Analog block, Power map (left), Thermal map (right)

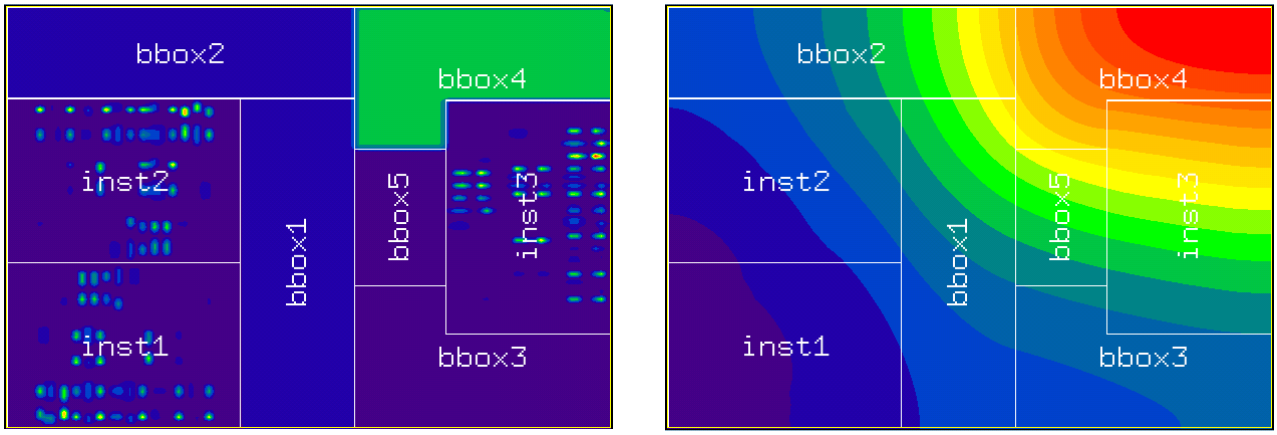
Temperature calculation for standalone analog block is based on power densities within this block and die/package parameters. With environment temperature of 25^{o}C, this die reports 27^{o}C average temperature and temperature spread of less than 0.25^{o}C. Traditional circuit simulation seems to be safe in this case.

Power and thermal maps for pseudo SoC design

There are three instances of the same analog layout in this design: **inst1**, **inst2,** and **inst3**. The rest of the design are black boxes with up to (±) 3 times difference in dissipated power.

Temperature Calculation for this "SoC" is based on total power numbers for blackboxes and calculated power for analog blocks. **It is important to note that power and temperature are calculated in the converging simulation process.**

This approach provides true accuracy compared to easy single step process of temperature calculation based on predefined power numbers.



Picture 4. Pseudo SoC, Power map (left), Thermal map (right)

Results of "SoC" analysis are different from single block analysis. Temperature variation across the block remains almost the same only for **inst1** while **inst3** has temperature variation of 1.2°C. Translated into temperature gradients, it results in impressive **18°C/mm**. With environment temperature of 25°C, this die reports 35.5°C average temperature (compare to 27°C for single block average) and temperature spread of 2.5°C. Temperature spread for most critical analog block increases in SoC environment almost 5 times compared to standalone analysis of this block.

Monte-Carlo models random variation well, but it is ineffective at analysis of systematic variation like temperature variation across the die. In this case, even if increasing the standard deviation, simulation will result in larger random variation but will very unlikely produce a temperature gradient. There are two issues:

a) overdesign for severe non-physical corners
b) underdesign for realizable scenarios.

Effects caused by packaging or die characteristics cannot be simulated using electrical circuit simulation alone. Temperature variation across the die is clearly systematic and requires a direct solution which Invarian offers. Rather than a random temperature variation or tightening of the parameters, it produces an accurate result with physically modeled temperature gradient.

Integrated analysis solution offered by Invarian helps designers to overcome existing analysis problems without additional flow complexity and runtime penalty.

Contacts:

Alex Samoylov
Invarian, Inc.
Phone: +1(408)834-5942
Email: ales@invarian.com
http://invarian.com

Mick Tegethoff
Berkeley Design® Automation, Inc.
Phone: +1(970)225-7971
Email: mick@berkeley-da.com
http://berkeley-da.com